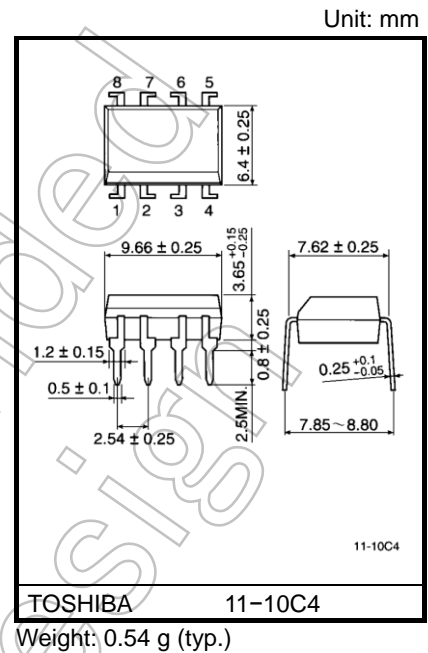


TLP651

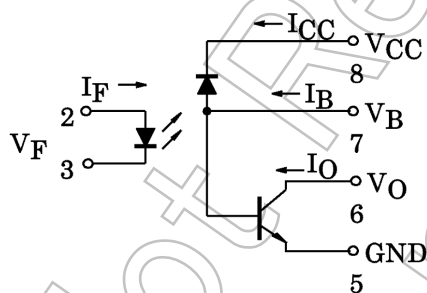
Digital Logic Ground Isolation
 Line Receiver
 Microprocessor System Interfaces
 Switching Power Supply Feedback Control
 Analog Signal Isolation

The TOSHIBA TLP651 consists of a GaAlAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.
 TLP651 has internal base connection. This base pin should be used for analog application or enable operation. If base pin is open, output signal will be noisy by environmental condition. For this case, TLP650 is suitable.

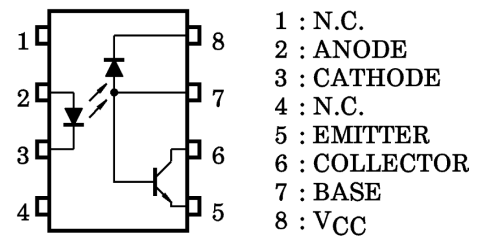
- Isolation voltage: 5000V_{rms} (min)
- Switching speed: t_{pHL} = 0.3μs (typ.)
 t_{pLH} = 0.5μs (typ.) (R_L = 1.9kΩ)
- TTL compatible
- UL recognized: UL1577, file no. E67349
- cUL approved :CSA Component Acceptance Service
 No. 5A, File No.E67349



Schematic



Pin Configuration (top view)



Start of commercial production
 1983-12

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	I _F	25	mA
	Pulse forward current (Note 2)	I _{FP}	50	mA
	Peak transient forward current (Note 3)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation (Note 4)	P _D	45	mW
Detector	Output current	I _O	8	mA
	Peak output current	I _{OP}	16	mA
	Output voltage	V _O	-0.5 to 15	V
	Supply voltage	V _{CC}	-0.5 to 15	V
	Base current	I _B	5	mA
	Emitter-base reverse voltage	V _{EB}	5	V
	Output power dissipation (Note 5)	P _O	100	mW
Operating temperature range		T _{opr}	-55 to 100	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead solder temperature (10s) (Note 6)		T _{sol}	260	°C
Isolation voltage (AC, 1minute, R.H.≤ 60%) (Note 7)		BV _S	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width.
Derate 1.6mA / °C above 70°C.

(Note 3) Pulse width ≤ 1μs, 300pps.

(Note 4) Derate 0.9mW / °C above 70°C.

(Note 5) Derate 2mW / °C above 70°C.

(Note 6) Soldering portion of lead: Up to 2mm from the body of the device.

(Note 7) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit	
LED	Forward voltage	V _F	I _F = 16mA	—	1.65	1.85	V	
	Forward voltage temperature coefficient	ΔV _F / ΔT _a	I _F = 16mA	—	-2	—	mV / °C	
	Reverse current	I _R	V _R = 5V	—	—	10	μA	
	Capacitance between terminal	C _T	V _F = 0 V, f = 1MHz	—	45	—	pF	
Detector	High level output current	I _{OH} (1)	I _F = 0mA, V _{CC} = V _O = 5.5V	—	3	500	nA	
		I _{OH} (2)	I _F = 0mA, V _{CC} = V _O = 15V	—	—	5	μA	
		I _{OH}	I _F = 0mA, V _{CC} = V _O = 15V Ta = 70°C	—	—	250	μA	
	High level supply voltage	I _{CCH}	I _F = 0mA, V _{CC} = 15V	—	0.01	1	μA	
Coupled	Current transfer ratio	I _O / I _F	I _F = 16mA V _{CC} = 4.5V V _O = 0.4V	Ta = 25°C	10	30	—	%
				Rank: O	19	30	—	
				Ta = 0 to 70°C	5	—	—	
	Rank: O	15	—	—				
Low level output voltage	V _{OL}	I _F = 16mA, V _{CC} = 4.5V, I _O = 1.1mA (Rank O: I _O = 2.4mA)	—	—	0.4	V		
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500VDC (Note 7)	5×10 ¹⁰	10 ¹⁴	—	Ω		
Capacitance between input to output	C _S	V _S = 0 V, f = 1MHz (Note 7)	—	0.8	—	pF		

Switching Characteristics (Ta = 25°C, Vcc = 5V)

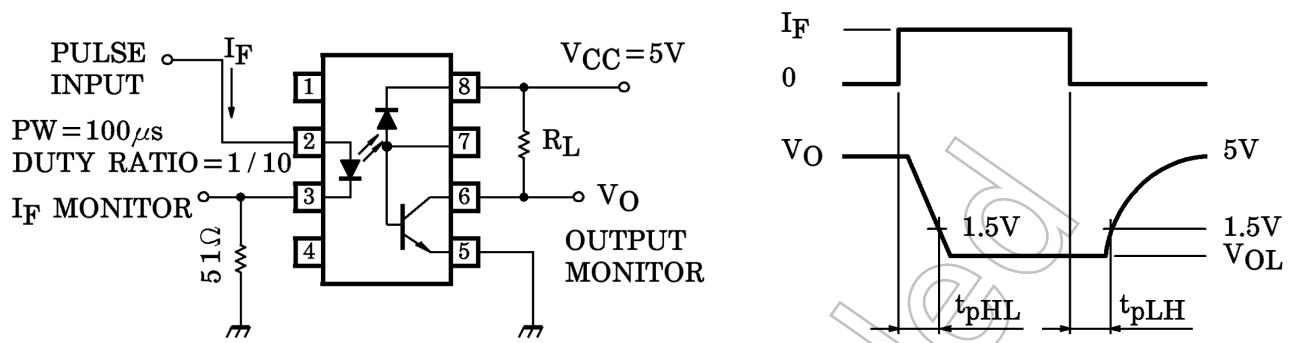
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	tpHL	1	I _F = 0→16mA	—	0.2	0.8	μs
			R _L = 4.1kΩ Rank O: R _L = 1.9kΩ	—	0.3	0.8	
Propagation delay time (L→H)	tpLH	1	I _F = 16→0mA	—	1.0	2.0	μs
			R _L = 4.1kΩ Rank O: R _L = 1.9kΩ	—	0.5	1.2	
Common mode transient immunity at logic high output (Note 8)	CMH	2	I _F = 0mA, V _{CM} = 200V _{p-p} R _L = 4.1kΩ (Rank O: R _L = 1.9kΩ)	—	400	—	V / μs
Common mode transient immunity at logic low output (Note 8)	CML		I _F = 16mA, V _{CM} = 200V _{p-p} R _L = 4.1kΩ (Rank O: R _L = 1.9kΩ)	—	-1000	—	V / μs

(Note 8) CML is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8V).

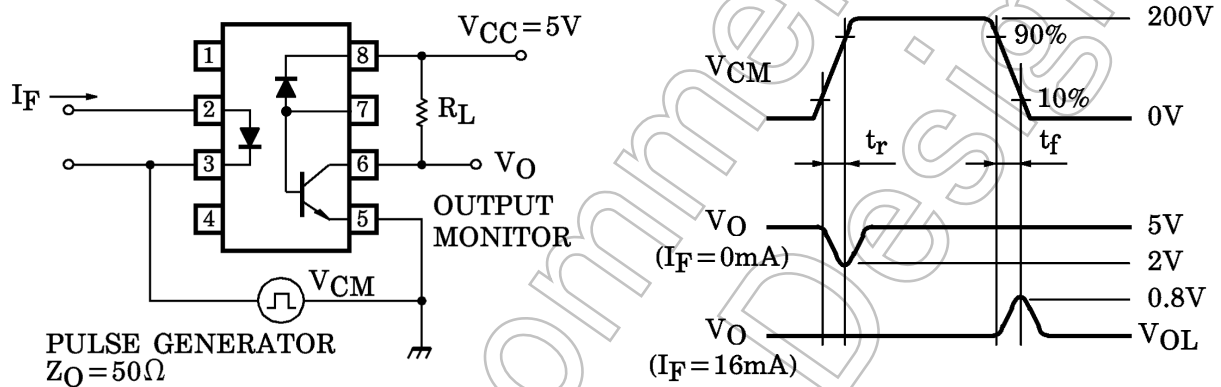
CMH is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0V).

Note: Maximum electrostatic discharge voltage for any pins: 100V (C = 200pF, R = 0).

Test Circuit 1: Switching Time Test Circuit

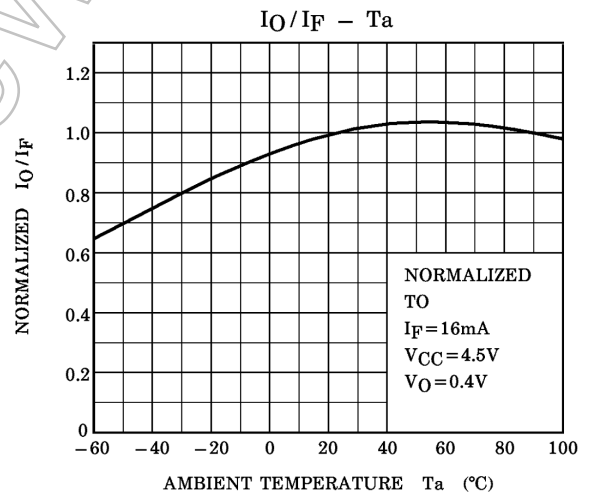
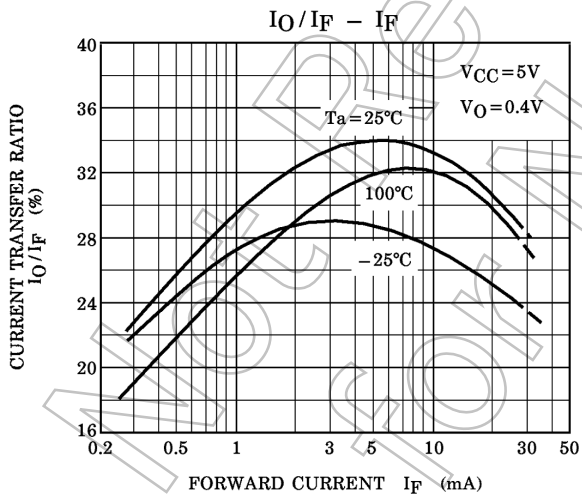
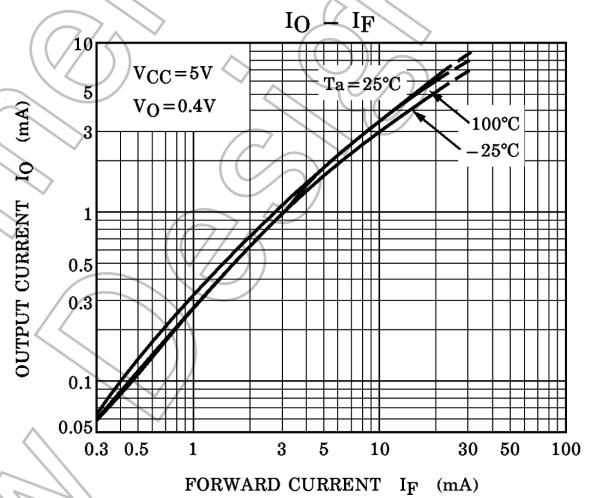
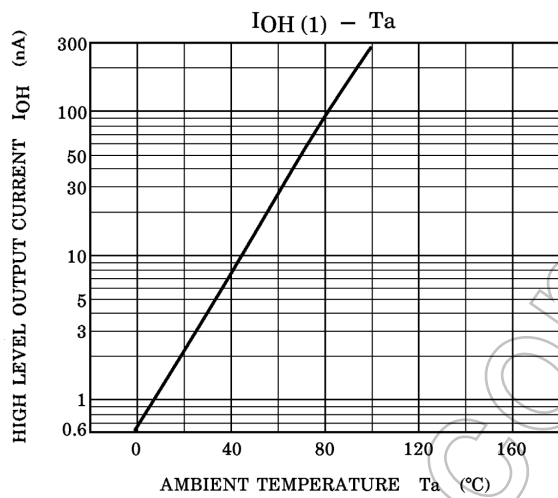
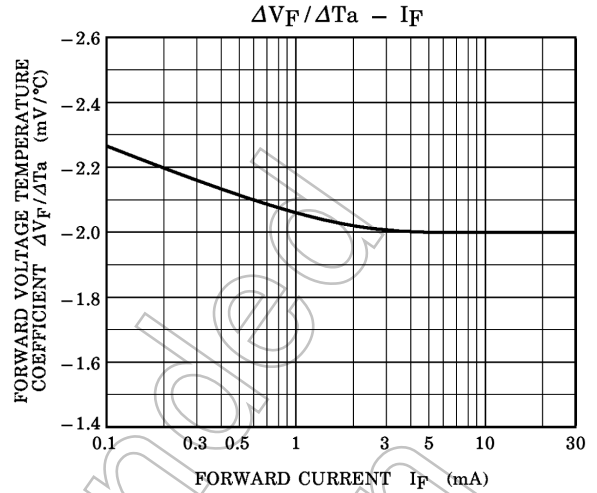
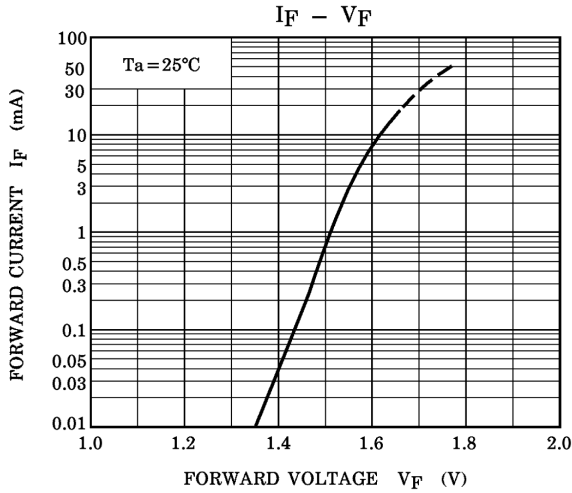


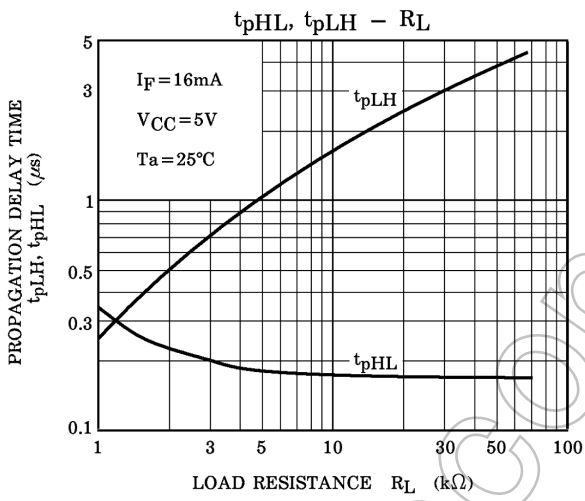
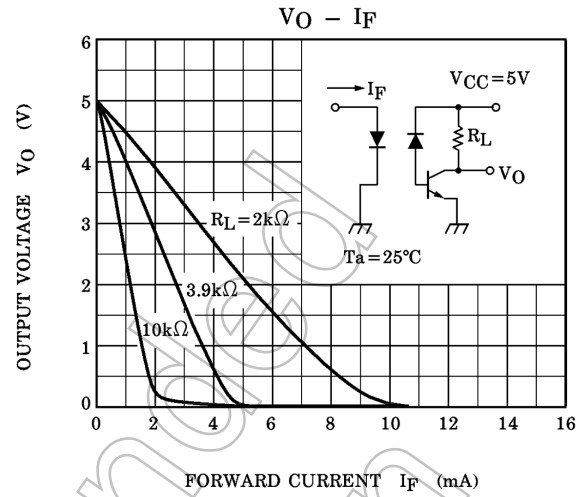
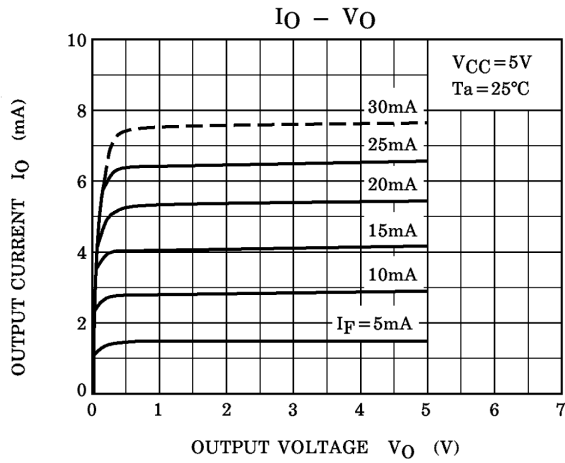
Test Circuit 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{160 (V)}{t_r (\mu s)}, \quad CM_L = \frac{160 (V)}{t_f (\mu s)}$$

Not Recommended for New





Not Recommended for New Design

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