TOSHIBA Photocoupler GaAℓAs IRED & Photo IC

TLP551

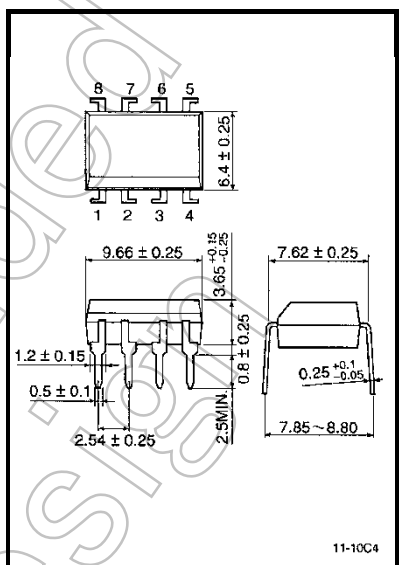
Controllers

Interfaces for Calculators and Control Devices

Noise Attenuation in Measurement and System Devices

Signal Transmission between circuits of different potential

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	11-10C4

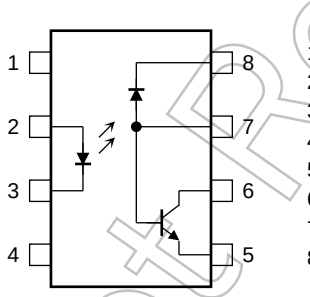
Weight: 0.54 g (typ.)

The TOSHIBA TLP551 consists of a GaAℓAs high-output light emitting diode and a high speed detector of one chip photo diode-transistor. This unit is 8-lead DIP.

TLP551 has an internal base connection. This base pin should be used for analog application or enable operation.

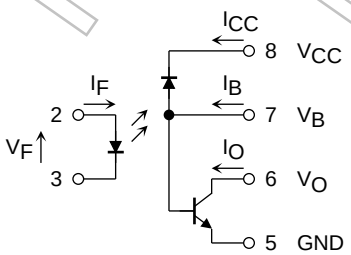
- Isolation voltage: 2500 V_{rms} (min)
- Switching speed: t_{pHL} = 0.5 μs (typ.)
  t_{pLH} = 0.6 μs (typ.)
  (R_L = 1.9 kΩ)
- TTL compatible
- If the base pin is open, external noise will cause interference to the output signal. In this scenario, TLP550 will be recommended.
- UL recognized: UL1577, file no. E67349
- cUL approved :CSA Component Acceptance Service
  No. 5A, File No.E67349

Pin Configurations (top view)



1: N.C.
2: Anode
3: Cathode
4: N.C.
5: Emitter
6: Collector
7: Base
8: V_{CC}

Schematic



Start of commercial production
1981-09

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	25	mA
	Forward current derating (Ta≥ 70 °C)	$\Delta I_F / \Delta Ta$	-0.8	mA/°C
	Pulse forward current (Note 1)	I_{FP}	50	mA
	Pulse forward current derating (Ta≥ 70 °C)	$\Delta I_{FP} / \Delta Ta$	-1.6	mA/°C
	Peak transient forward current (Note 2)	I_{FPT}	1	A
	Reverse voltage	V_R	5	V
	Diode power dissipation	P_D	45	mW
	Diode power dissipation derating (Ta ≥ 70 °C)	$\Delta P_D / \Delta Ta$	-0.9	mW/°C
Detector	Output current	I_O	8	mA
	Peak output current	I_{OP}	16	mA
	Output voltage	V_O	−0.5 to 15	V
	Supply voltage	V_{CC}	−0.5 to 15	V
	Base current	I_B	5	mA
	Emitter-base reverse voltage	V_{EB}	5	V
	Output power dissipation	P_O	100	mW
	Output power dissipation derating (Ta≥ 70 °C)	$\Delta P_O / \Delta Ta$	-1.8	mW/°C
Operating temperature range		T_{opr}	−55 to 100	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Lead solder temperature (10 s) (Note 3)		T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60%) (Note 4)		BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50% duty cycle, 1 μs pulse width.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: Soldering portion of lead: up to 2 mm from body of the device.

Note 4: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

	Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
LED	Forward voltage	V_F	I_F = 16 mA	1.45	1.65	1.85	V
	Forward voltage temperature coefficient	$\Delta V_F/\Delta Ta$	I_F = 16 mA	—	−2	—	mV/°C
	Reverse current	I_R	V_R = 5 V	—	—	10	μA
	Capacitance between terminal	C_T	V_F = 0 V, f = 1 MHz	—	60	—	pF
Detector	High level output current	$I_{OH(1)}$	I_F = 0 mA, V_{CC} = V_O = 5.5 V	—	3	500	nA
		$I_{OH(2)}$	I_F = 0 mA, V_{CC} = V_O = 15 V	—	—	5	μA
		I_{OH}	I_F = 0 mA, V_{CC} = V_O = 15 V, Ta = 70°C	—	—	50	μA
	High level supply voltage	I_{CCH}	I_F = 0 mA, V_{CC} = 15 V	—	0.01	1	μA

Coupled Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		Min	Typ.	Max	Unit
Current transfer ratio	I_O/I_F	I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.4 V		10	30	—	%
			Rank: O	19	30	—	
		I_F = 16 mA, V_{CC} = 4.5 V, V_O = 0.4 V		5	—	—	
		Ta = 0 to 70°C	Rank: O	15	—	—	
Low level output voltage	V_{OL}	I_F = 16 mA, V_{CC} = 4.5 V, I_O = 1.1 mA (Rank O: I_O = 2.4 mA)		—	—	0.4	V

Isolation Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance (input-output)	C_S	V_S = 0 V, f = 1 MHz	—	0.8	—	pF
Resistance (input-output)	R_S	V_S = 500 V_{DC}, R.H. ≤ 60% (Note 1)	5×10^{10}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 60 s	2500	—	—	V_{rms}
		AC, 1 s, in oil	—	5000	—	
		DC, 60 s, in oil	—	5000	—	V_{dc}

Note 1: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, V_{CC} = 5 V)

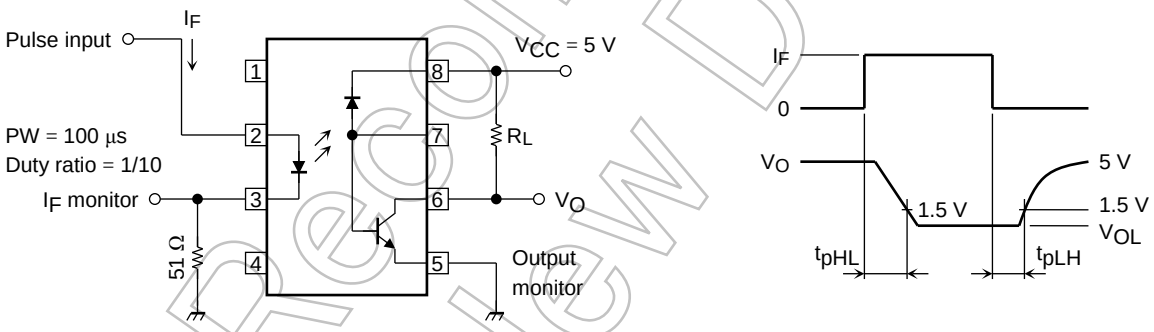
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H → L)	t_{pHL}	1	I_F = 16 mA, R_L = 4.1 kΩ	—	0.3	0.8	μs
			I_F = 16 mA, R_L = 1.9 kΩ (Rank O)	—	0.5	0.8	
Propagation delay time (L → H)	t_{pLH}	1	I_F = 16 mA, R_L = 4.1 kΩ	—	1	2	μs
			I_F = 16 mA, R_L = 1.9 kΩ (Rank O)	—	0.6	1.2	
Common mode transient immunity at logic high output	CM_H	2	I_F = 0 mA, V_{CM} = 200 V_{p-p} R_L = 4.1 kΩ (Rank O: R_L = 1.9 kΩ)	—	400	—	V/μs
Common mode transient immunity at logic low output	CM_L	2	I_F = 16 mA, V_{CM} = 200 V_{p-p} R_L = 4.1 kΩ (Rank O: R_L = 1.9 kΩ)	—	−1000	—	V/μs

Note: CM_H: The maximum tolerable rate of rise of the common mode voltage to ensure that the output will remain in the high output state (i.e., V_O > 2.0 V). Measured in volts per microsecond (V/μs).

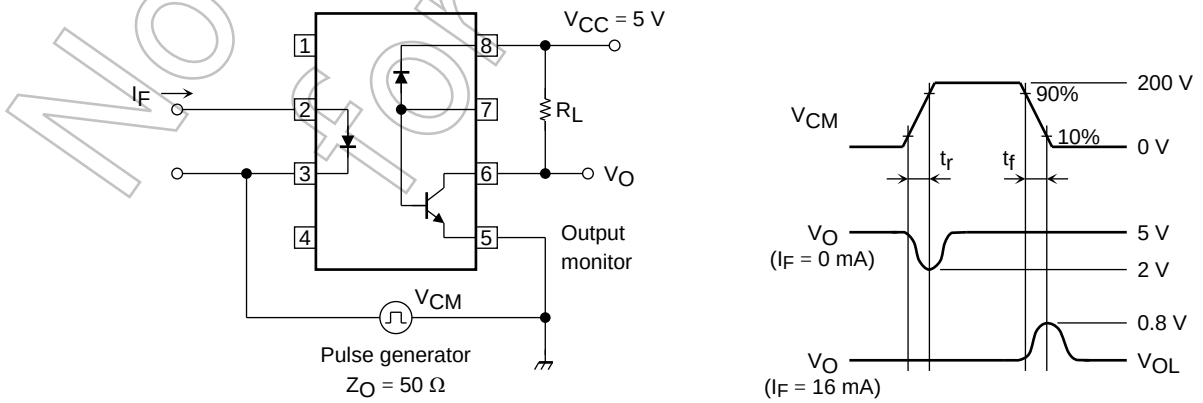
CML: The maximum tolerable rate of fall of the common mode voltage to ensure that the output will remain in the low output state (i.e., V_O < 0.8 V). Measured in volts per microsecond (V/μs).

Maximum electrostatic discharge voltage for any pins: 100 V (C = 200 pF, R = 0).

Test Circuit 1: Switching Time Test Circuit

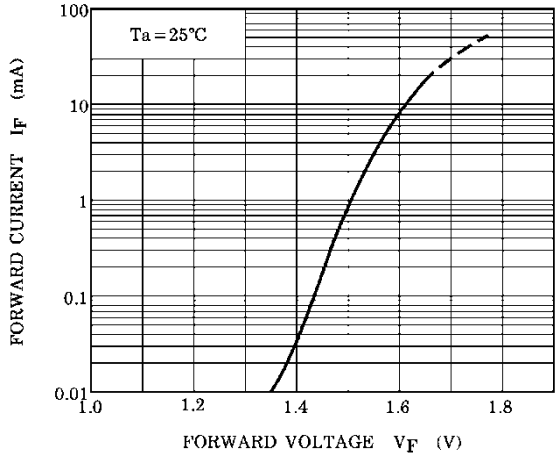


Test Circuit 2: Common Mode Noise Immunity Test Circuit

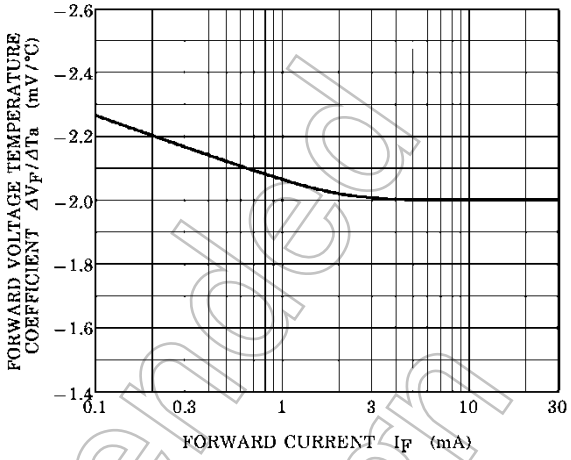


$$CM_H = \frac{160\ (V)}{t_r\ (\mu s)},\ CM_L = \frac{160\ (V)}{t_f\ (\mu s)}$$

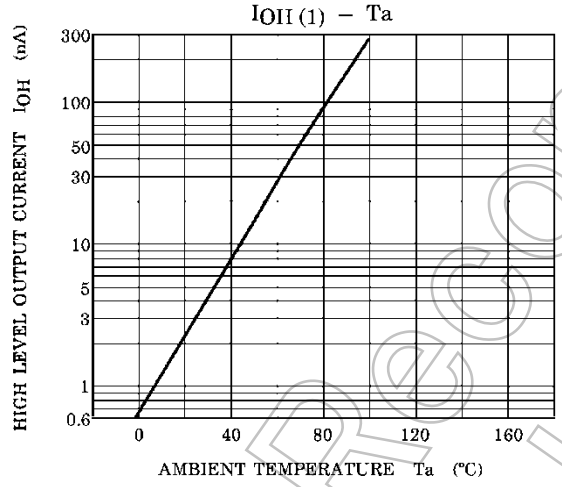
$I_F - V_F$



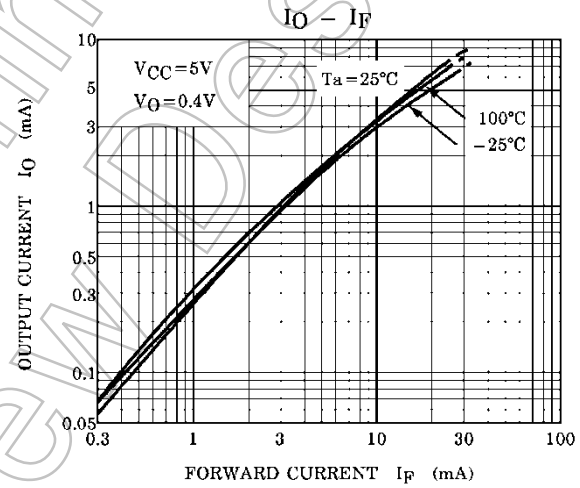
$\Delta V_F / \Delta Ta - I_F$



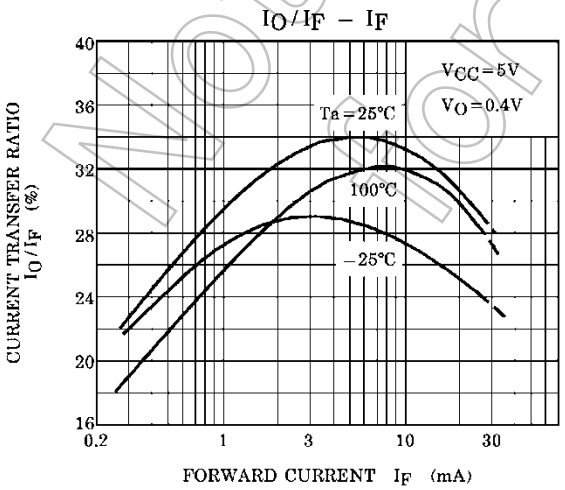
$I_{OH}\,(1) - Ta$



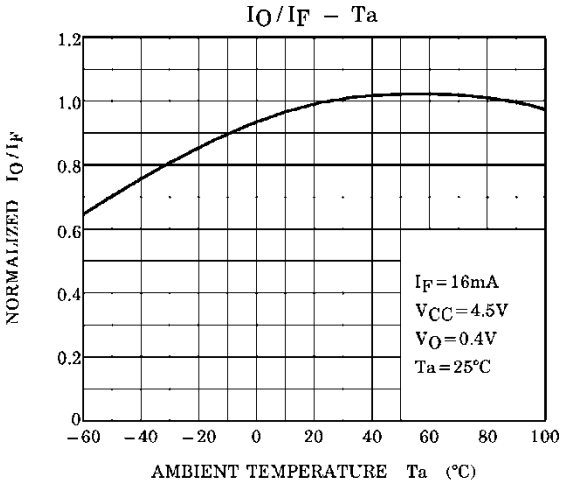
$I_O - I_F$



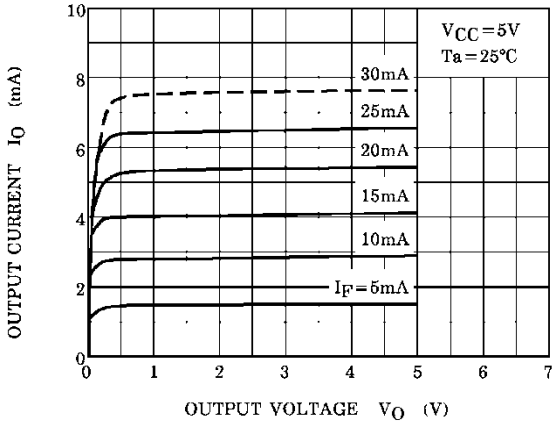
$I_O / I_F - I_F$



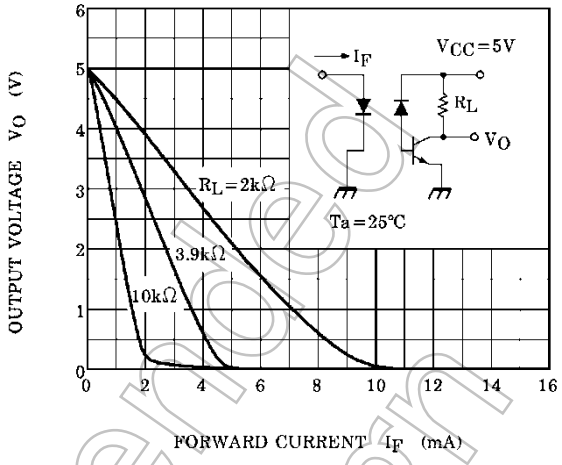
$I_O / I_F - Ta$



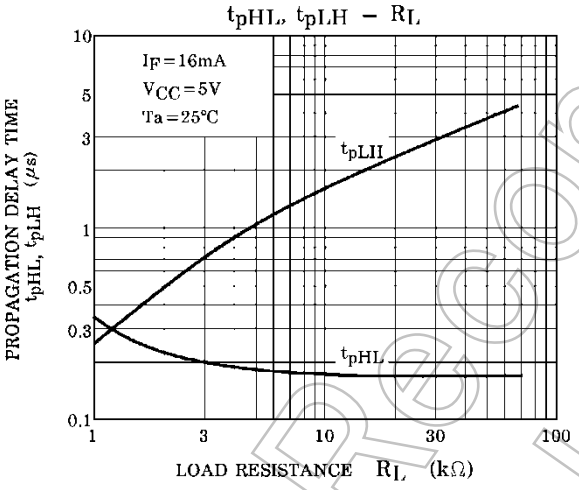
$I_O - V_O$



$V_O - I_F$



t_{pHL}, $t_{pLH} - R_L$



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